I Claim:

1. In a general purpose computer system incorporating at least one CPU and associated cache in communication with a CPU bus, at least one I/O device in communication with at least one I/O bus, the at least one CPU and associated cache and the at least one I/O device are all in communication with a shared memory, the communication provided by a system controller having CPU interface logic and I/O interface logic and having a plurality of operational modes, a method for processing I/O transactions between the at least one I/O device and the shared memory comprising:

A) assigning first and second memory address ranges to the at least one I/O bus;

B) programming the CPU interface logic to respond to all addresses that correspond to shared memory;

C) programming the CPU cache to only store data corresponding to one of the memory address ranges;

D) programming the system controller to distinguish between the first and the second memory address ranges and to operate in a first mode if the system controller detects an I/O request address corresponding to the first memory address range and to operate in a second mode if the system controller detects an I/O request address corresponding to the second memory address range;

E) receiving at the system controller an I/O request from the at least one I/O device; and

F) forwarding the I/O request to the shared memory if the system controller is operating in the first mode and to the CPU bus if the system controller is operating in the second mode.

2. The method of claim 1, wherein the first memory address range corresponds to an I/O transaction processed in a non-coherent manner and the second memory address range corresponds to an I/O transaction processed in a coherent manner.

3. The method of claim 1, wherein the cache is programmed to store data corresponding to the second memory address range.

4. The method of claim 1, wherein the first and second memory address ranges are different sizes.

5. The method of claim 1, wherein the first and second memory address ranges are the same size.

6. The method of claim 1, wherein the first operation mode processes the I/O request non-coherently and the second operation mode processes the I/O request coherently.

7. The method of claim 1, wherein the step of programming the system controller includes setting an I/O address decoder on the system controller.

8. The method of claim 1, wherein the at least one I/O bus is a processor bus.

9. In a general purpose computer system incorporating at least one CPU and associated cache in communication with a CPU bus, at least one I/O device in communication with at least one I/O bus, the at least one CPU and associated cashe and the at least one I/O device are all in communication with a shared memory, the communication provided by a system controller having CPU interface logic and I/O interface logic, a method for processing I/O transactions between the at least one I/O device and the shared memory in a coherent manner comprising the steps of:

A) assigning a memory address range to the I/O bus;

B) programming the CPU interface logic to respond to all addresses that correspond to shared memory;

C) programming the CPU cache to store data corresponding to the assigned memory address range;

D) programming the system controller to detect I/O requests in the assigned memory address range and to operate in a coherent mode if the the system controller detects an I/O request in the assigned memory address range;

E) receiving at the system controller an I/O request from the I/O device; and

F) forwarding the I/O request to the CPU bus.

10. The method of processing I/O transactions in claim 9, wherein the I/O request corresponds to the assigned memory address range.

11. The method of processing I/O transactions in claim 9, wherein the step of setting the system controller includes programming the I/O address decoder so that the memory address range selects the CPU master unit.

12. In a general purpose computer system incorporating at least one CPU and associated cache in communication with a CPU bus, at least one I/O device and at least one CPU both in communication with a processor bus, the at least one CPU and associated cache and the at least one I/O device are all in communication with a shared memory, the communication provided by a system controller having CPU interface logic and processor bus interface logic and having a plurality of operational modes, a method for processing I/O transactions between the at least one I/O device and the shared memory comprising:

A) assigning first and second memory address ranges to the processor bus;

B) programming the CPU interface logic to respond to all addresses that correspond to shared memory;

C) programming the CPU cache to only store data corresponding to one of the memory address ranges;

D) programming the system controller to distinguish between the first and the second memory address ranges and to operate in a first mode if the system controller detects an I/O request address corresponding to the first memory address range and to operate in a second mode if the system controller detects an I/O request address corresponding to the second memory address range;

E) receiving at the system controller an I/O request from the at least one I/O device; and

F) forwarding the I/O request directly to the shared memory if the system controller is operating in the first mode and directly to the CPU bus if the system controller is operating in the second mode.

13. The method of claim 12, wherein the first memory address range corresponds to an I/O transaction processed in a non-coherent manner and the second memory address range corresponds to an I/O transaction processed in a coherent manner.

14. The method of claim 12, wherein the cache is programmed to store data corresponding to the second memory address range.

15. The method of claim 12, wherein the first and second memory address ranges are different sizes.

16. The method of claim 12, wherein the first and second memory address ranges are the same size.

17. The method of claim 12, wherein the first operation mode processes the I/O request non-coherently and the second operation mode processes the I/O request coherently.

18. The method of claim 12, wherein the step of programming the system controller includes setting a PCI target address decoder on the system controller.